Data Centers and High Performance Computing
July 14th, 2016

Name: _____ **Surname**: _____ **Student ID**: _____

Remember to write your correct personal data on this sheet, and use it as a folder to wrap the exposition. If you think a question is ambiguous, write your interpretation and answer accordingly. You are not allowed to use any note or digital device. If you are found copying or consulting notes, you will not pass the written test.

Question 1 - (9 points)
Discuss the possible advantages of a computing architecture without cache coherency.
Consider a possible computing architecture wth only one level of cache, without any cache coherency guarantee. Suppose that, in such a computing architecture, the Instruction Set offers the primitive [illegible], which forces a write back of the cache line where [illegible] falls in.
Write a possible implementation (in pseudocode) of a spinlock primitive composed of two API functions: i) [illegible], which allows to acquire a lock if no other process has already acquired it, and ii) [illegible], which releases the lock.

Question 2 - (5 points)
Discuss the role of the scheduler in the the context of liveness condition of concurrent programs.

Question 3 - (5 points)
Describe differences, limits, advantages and disadvantages of Software vs. Hardware Transactional Memory.

Question 4 - (7 points)
Discuss in what cases a deadlock might arise in a program based on MPI, when two or more ranks exchange data using send and receive primitives. What is a possible solution to it?

Question 5 - (5 points)
Discuss the problem related to the convergence of continuous simulation in case it is realized via forward differences computed according to a certain time step.

I, the undersigned, according to the provisions of law N. 675/96, allow the teachers to publish on the website the results of this written test.

Legible signature in full: _____